Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously presented) A configurable interface circuit comprising:

a first internal circuit operable to provide a first internal signal via a first internal signal path;

an input buffer operable to receive a first external signal via a first external signal path;

a selector circuit coupled to the first internal circuit via the first internal signal path, and to the input buffer, the selector circuit operable to select either the first internal signal or the first external signal to provide a selected signal;

an output buffer operative to receive a second internal signal via a second internal signal path and to provide the second internal signal via the first external signal path; and

a second internal circuit operable to provide the second internal signal via the second internal signal path and to receive the selected signal via a third internal signal path, the selector circuit inoperable to receive the second internal signal.

2. (Canceled)

3. (Original) The configurable interface circuit of Claim 1, wherein:

the first internal signal path and the first external signal path are operable to propagate signals in accordance with a common protocol.

4. (Original) The configurable interface circuit of Claim 3, wherein:

protocol is a PCI bus protocol.

5. (Original) The configurable interface circuit of Claim 3, wherein: protocol is an AGP bus protocol.

6. (Original) The configurable interface circuit of Claim 3, wherein: protocol is an NGP bus protocol.

7. (Canceled)

8. (Previously presented) The configurable interface circuit of Claim 1, wherein: the second internal circuit is operable to provide the second internal signal via the second internal signal path to both the first internal circuit and the output buffer.

9. (Previously presented) The configurable interface circuit of Claim 1, wherein: the second internal circuit is operable to receive a selected signal that is either the first internal signal or the first external signal from the selector circuit, and inoperable to receive the second internal signal from the selector circuit.

10. (Previously presented) The configurable interface circuit of Claim 1, wherein: the second internal circuit is operable to provide the second internal signal to the first internal circuit via a fourth internal signal path when the second internal circuit is in a first mode, and to provide the second internal signal to the output buffer via the second internal signal path when the second internal circuit is in a second mode.

11. (Previously presented) The configurable interface circuit of Claim 1, wherein:

the second internal circuit comprises a bus interface.

12. (Original) The configurable interface circuit of Claim 11, wherein:

the second internal circuit is a bus bridge.

13. (Original) The configurable interface circuit of Claim 1, wherein:

the first internal circuit comprises a bus interface.

14. (Original) The configurable interface circuit of Claim 11, wherein:

the first internal circuit is a graphics controller.

15. (Previously presented) The configurable interface circuit of Claim 1, wherein:

the first internal circuit is operable to receive the second internal signal via the second internal signal path.

16. (Previously presented) The configurable interface circuit of Claim 1, further comprising:

a bus bridge, comprising a bus interface, operable to provide a second internal signal to the first internal circuit via a second internal signal path and to receive the selected signal via a third internal signal path.

17. (Original) The configurable interface circuit of Claim 16, wherein:

the first internal signal path and the first external signal path are operable to propagate signals in accordance with a common protocol.

18. (Original) The configurable bus interface circuit of Claim 1, wherein:

the selector circuit is operable to provide a selected signal that is uncorrupted by transmission line effects.

19. (Original) The configurable bus interface circuit of Claim 1, wherein:

the input buffer is inoperable to provide the first external signal from the first external signal path to the first internal circuit.

20. (Previously presented) The configurable bus interface circuit of Claim 1, wherein:

the input buffer is inoperable to provide the first external signal from the first external signal path to the first internal circuit; and

the output buffer is inoperable to provide the first external signal from the first external signal path to the first internal circuit.

21. (Currently amended) A method for configuring a bus interface circuit comprising:

at an ~~internal~~ on chip circuit, receiving a bus bridge signal from an ~~internal~~ on chip bus bridge; and

at an ~~internal~~ on chip I/O circuit, preventing signals from any ~~external~~ off chip circuit from reaching the internal circuit.

22. (Currently amended) The method of Claim 21, further comprising:

at the ~~external~~ off chip circuit, receiving the bus bridge signal from the ~~internal~~ on chip bus bridge; and

at the ~~external~~ off chip circuit, reflecting the bus bridge signal to the internal I/O circuit.

23. (Currently amended) The method of Claim 21, further comprising:

at the bus bridge, receiving an ~~internal~~ on chip circuit signal from the ~~internal~~ on chip circuit;

at the ~~internal~~ on chip I/O circuit, receiving an ~~external~~ off chip circuit signal from the ~~external~~ off chip circuit;

at the bus bridge, receiving the ~~external~~ off chip circuit signal; and

at the bus bridge, selecting one of the ~~internal~~ on chip circuit signal and the ~~external~~ off chip circuit signal.

24. (Original) The method of Claim 23, wherein:

selecting includes multiplexing.

25. (Original) The method of Claim 21, wherein:

receiving a bus bridge signal from the bus bridge is without input buffering.

26. (Original) The method of Claim 21, wherein:

receiving a bus bridge signal from the bus bridge comprises receiving a signal that is operably compatible with a PCI bus.

27. (Original) The method of Claim 21, wherein:

receiving a bus bridge signal from the bus bridge comprises receiving a signal that is operably compatible with an AGP bus.

28. (Original) The method of Claim 21, wherein:

receiving a bus bridge signal from the bus bridge comprises receiving a signal that is operably compatible with an NGP bus.

29. (Currently amended) A computer system comprising:

a processing unit coupled to a processor bus;

a memory unit coupled to a memory bus; and

an integrated bus bridge graphics unit, coupled to the memory bus and further operably coupled to provide a signal to an external graphics bus, the integrated bus bridge graphics unit comprising an ~~internal~~ on chip circuit operably configured to avoid signals from the ~~external~~ off chip graphics bus.

30. (Currently amended) The computer system of Claim 29, wherein:

the integrated bus bridge graphics unit is further operably coupled to receive a signal from the ~~external~~ off chip graphics bus via an ~~internal~~ on chip I/O circuit.

31. (Currently amended) The computer system of Claim 29, wherein:

the integrated bus bridge graphics unit is further configurable to select, and to provide a signal to, one of the ~~internal~~ on chip circuit and the ~~external~~ off chip graphics bus, and is further operably configured to isolate the ~~internal~~ on chip circuit from an ~~external~~ off chip graphics bus signal.

32. (Currently amended) The computer system of Claim 29, wherein:

the integrated bus bridge graphics unit is further configurable to select, and to receive a signal from, one of the ~~internal~~ on chip circuit and the ~~external~~ off chip graphics bus.

33. (Currently amended) The computer system of Claim 29, wherein:

the integrated bus bridge graphics unit is further operably configured to receive an ~~external~~ off chip signal from the ~~external~~ off chip graphics bus and to isolate the ~~internal~~ on chip circuit from the ~~external~~ off chip signal.

34. (Original) The computer system of Claim 33, wherein:

the integrated bus bridge graphics unit is further operably configured to receive an external signal via an input buffer from an external circuit, and to isolate the external signal.

35. (Original) The computer system of Claim 29, wherein:

the integrated bus bridge graphics unit is operably configured to provide signals to the internal circuit bufferlessly.

36. (Original) The computer system of Claim 29, wherein:

the integrated bus bridge graphics unit is operably configured to provide signals to the internal circuit uncorrupted by transmission line effects.

37. (Original) The computer system of Claim 29, wherein:

the internal circuit is operably coupled to receive signals that are compatible with a PCI bus.

38. (Original) The computer system of Claim 29, wherein:

the internal circuit is operably coupled to receive signals that are compatible with an AGP bus.

39. (Original) The computer system of Claim 29, wherein:

the internal circuit is operably coupled to receive signals that are compatible with an NGP bus.

40. (Previously presented) A configurable interface circuit comprising:

an internal graphics controller operable to provide a first internal signal via a first internal signal path;

an input buffer operable to receive a first external signal via a first external signal path;

a selector circuit coupled to the internal graphics controller via the first internal signal path, and to the input buffer, the selector circuit operable to select either the first internal signal or the first external signal to provide a selected signal;

a bus bridge, comprising a bus interface, operable to provide a second internal signal to the internal graphics controller via a second internal signal path and to receive the selected signal via a third internal signal path; and

an output buffer operative to receive the second internal signal via the second internal signal path and to provide the second internal signal via the first external signal path such that the input buffer and the selector circuit are inoperable to receive the second internal signal.

41. (Previously presented) A configurable bus interface circuit comprising:

a first internal circuit operable to provide a first internal signal via a first internal signal path;

an input buffer, operatively coupled to a first external signal path, and to the first internal circuit via the first internal signal path, and operative to receive the first internal signal from the first internal signal path and to provide the first external signal on the first external signal path; and

a selector circuit, operatively coupled to the first internal circuit via the first internal signal path, and to the input buffer, and operative to cause the input buffer to provide the first internal signal from the first internal signal path to the first external signal path, and to isolate the first internal signal on the first internal signal path from the first external signal.

42. (Previously presented) The configurable bus interface circuit of claim 41 including:

a first external circuit, operatively coupled to the input buffer via the first external signal path to receive the first external signal, such that the input buffer is operative to provide the first internal signal from the first internal signal path to the first external signal path, and to prevent the first internal signal on the first internal signal path from propagating to the first external signal path.

43. (Previously presented) The configurable bus interface circuit of claim 41 wherein the first external circuit is a vacant expansion slot such that the input buffer prevents the first internal signal on the first internal signal path from propagating onto the first external signal path.

44. (Previously presented) A configurable bus interface circuit comprising:

a first internal circuit operable to provide a first internal signal via a first internal signal path;

an input buffer, operatively coupled to a first external signal path, and to the first internal circuit via the first internal signal path, and operative to receive the first internal signal from the first internal signal path and to provide the first external signal on the first external signal path;

a selector circuit, operatively coupled to the first internal circuit via the first internal signal path, and to the input buffer, and operative to cause the input buffer to provide the first internal signal from the first internal signal path to the first external signal path, and to isolate the first internal signal on the first internal signal path from the first external signal;

an output buffer operative to receive a second internal signal via a second internal signal path and to provide the second internal signal via the first external signal path; and

a second internal circuit operable to provide the second internal signal via the second internal signal path and to receive the selected signal via a third internal signal path, the selector circuit inoperable to receive the second internal signal.

45. (Previously presented) The configurable bus interface circuit of claim 44 including:

a first external circuit, operatively coupled to the input buffer via the first external signal path to receive the first external signal, such that the input buffer is operative to provide the first internal signal from the first internal signal path to the first external signal path, and to prevent the first internal signal on the first internal signal path from propagating to the first external signal path.